

What is claimed is:

Sub B1

1. A method for forming gate electrodes of a semiconductor device, the method comprising:

- forming a gate insulation layer over a semiconductor wafer;
- forming a conductive layer over the gate insulation layer;
- forming a low-dielectric layer over the conductive layer;
- forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;
- patterning the low-dielectric layer using the photoresist pattern as a mask;
- removing the photoresist pattern;
- shrinking the low-dielectric pattern; and
- forming gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask.

2. The method of claim 1, wherein the low-dielectric layer is formed of an organic spin-on-glass layer or inorganic spin-on-glass layer.

Sub B2

3. The method of claim 1 or 2, wherein forming the low-dielectric layer comprises:

- depositing a low-dielectric layer over the conductive layer for the gate electrodes; and
- soft-baking the low-dielectric layer at a predetermined temperature.

4. The method of claim 1, wherein shrinking the low-dielectric pattern includes curing the low-dielectric pattern at a temperature of 400-500°C.

5. The method of claim 1, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time.

B

Sub A1

6. A method for forming fine patterns of a semiconductor device, the method comprising:
forming a material layer over a semiconductor wafer;
forming a low-dielectric layer over the material layer;
forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;
patterning the low-dielectric layer using the photoresist pattern as a mask;
removing the photoresist pattern;
shrinking the low-dielectric pattern; and
forming the fine patterns by patterning the material layer using the shrunken low-dielectric pattern as a mask.

7. The method of claim 6, wherein the low-dielectric layer is formed of an organic spin-on-glass layer or inorganic spin-on-glass layer. B

Sub A2

8. The method of claim 6 or 7, wherein forming the low-dielectric layer comprises:
depositing a low-dielectric layer over the material layer for the fine patterns;
and
soft-baking the low-dielectric layer at a predetermined temperature.

9. The method of claim 6, wherein shrinking the low-dielectric pattern further includes curing the low-dielectric pattern at a temperature of 400-500°C. B

10. The method of claim 9, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time.

Add B3